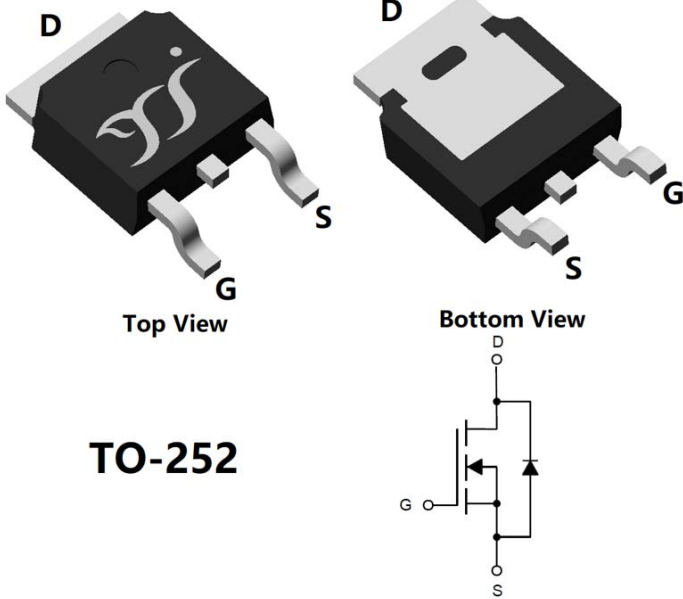


## N-Channel Enhancement Mode Field Effect Transistor



**TO-252**

### Product Summary

- $V_{DS}$  20V
- $I_D$  60A
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) <6.0mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=2.5V$ ) <8.8mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=1.8V$ ) <14mohm
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	20	V
Gate-source Voltage		$V_{GS}$	$\pm 10$	V
Drain Current	$T_C=25^\circ C$	$I_D$	60	A
	$T_C=100^\circ C$		38	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	210	A
Total Power Dissipation	$T_C=25^\circ C$	$P_D$	29	W
	$T_C=100^\circ C$		11	
Single Pulse Avalanche Energy <sup>B</sup>		$E_{AS}$	68	mJ
Thermal Resistance Junction-to-Case <sup>C</sup>		$R_{\theta JC}$	4.3	$^\circ C/W$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD60N02A	F1/F2	YJD60N02A	2500	/	25000	13" reel



# YJD60N02A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> =20A		4.5	6.0	mΩ
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> =15A		5.5	8.8	
		V <sub>GS</sub> = 1.8V, I <sub>D</sub> =10A		8.0	14	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				60	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> = 0V, f= 1MHZ		2250		pF
Output Capacitance	C <sub>oss</sub>			334		
Reverse Transfer Capacitance	C <sub>rss</sub>			271		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 10V, I <sub>D</sub> = 15A		27.9		nC
Gate-Source Charge	Q <sub>gs</sub>			4.1		
Gate-Drain Charge	Q <sub>gd</sub>			7.4		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 15A, di/dt= 100A/us		2.2		
Reverse Recovery Time	t <sub>rr</sub>			16.3		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> = 4.5V, V <sub>DD</sub> = 10V, I <sub>D</sub> = 10A, R <sub>L</sub> = 1Ω R <sub>GEN</sub> = 3Ω		13		ns
Turn-on Rise Time	t <sub>r</sub>			53		
Turn-off Delay Time	t <sub>D(off)</sub>			61		
Turn-off fall Time	t <sub>f</sub>			76		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=18V, V<sub>G</sub>=5V, L=0.5mH, R<sub>g</sub>=25Ω, I<sub>AS</sub>=16.5A

C. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the soldermounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

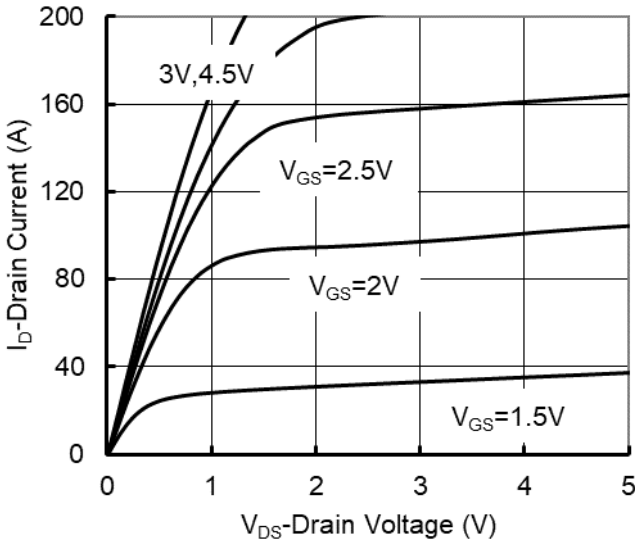


Figure1. Output Characteristics

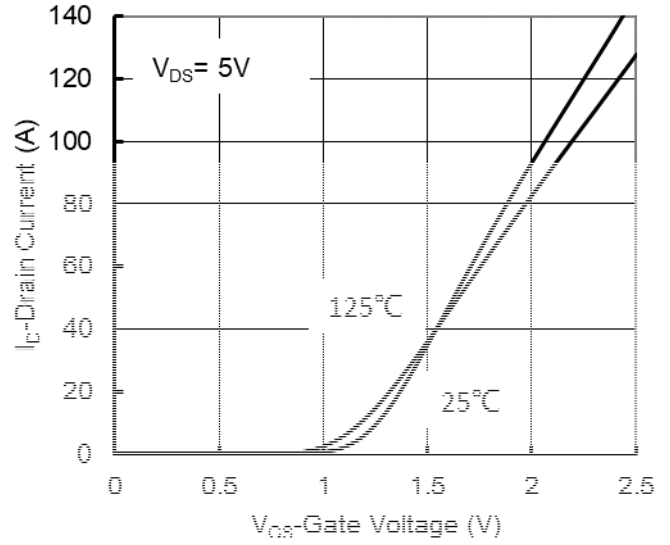


Figure2. Transfer Characteristics

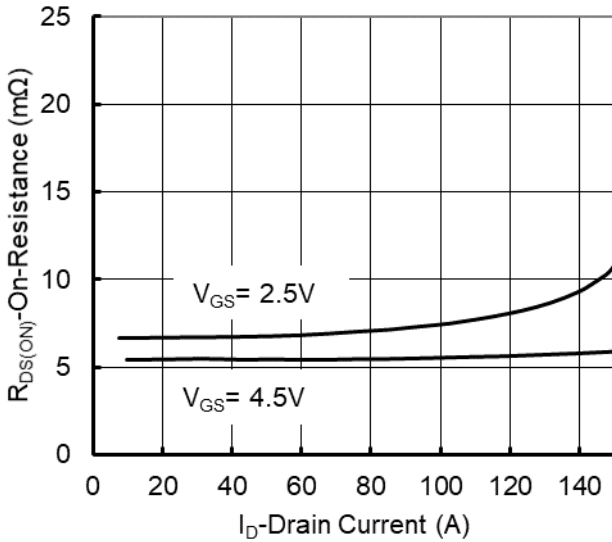


Figure3. On-Resistance vs. Drain Current

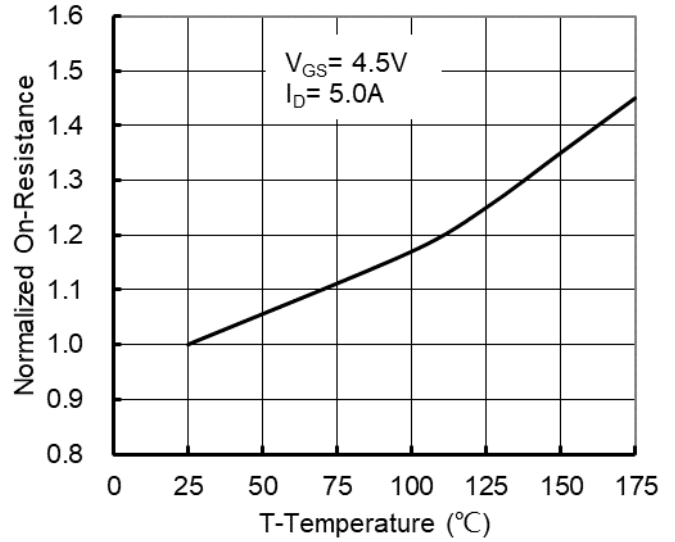


Figure4. Gate Charge

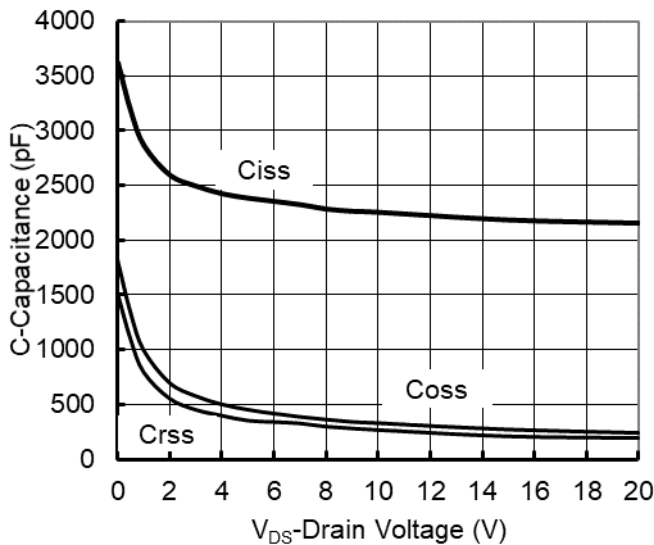


Figure5. Capacitance Characteristics

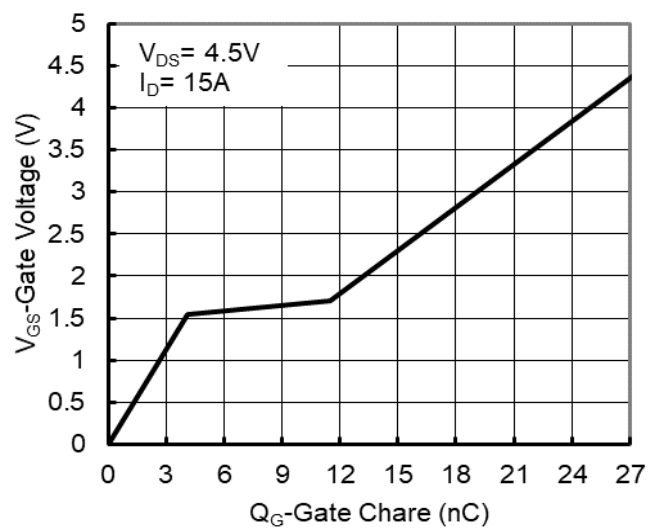


Figure6. Gate Charge



# YJD60N02A

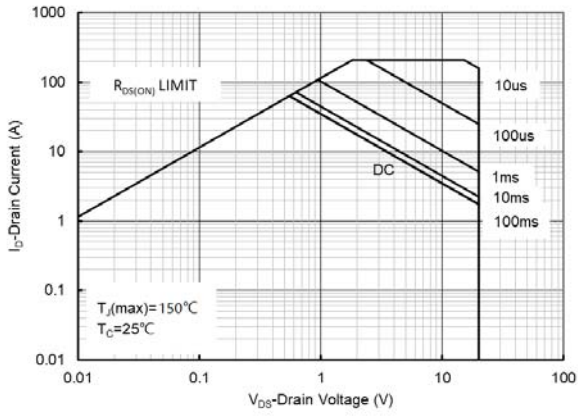


Figure7. Safe Operation Area

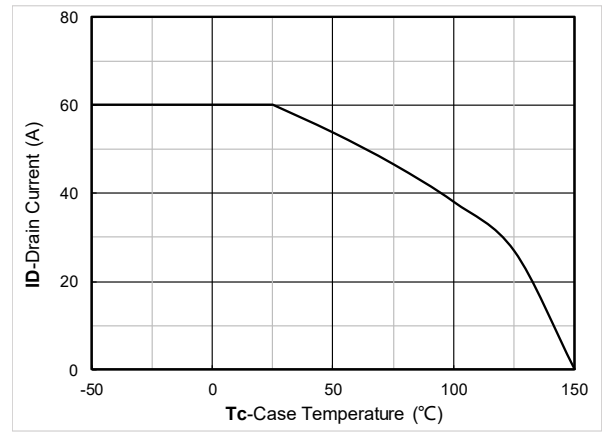


Figure8. Maximum Continuous Drain Current vs. Case Temperature

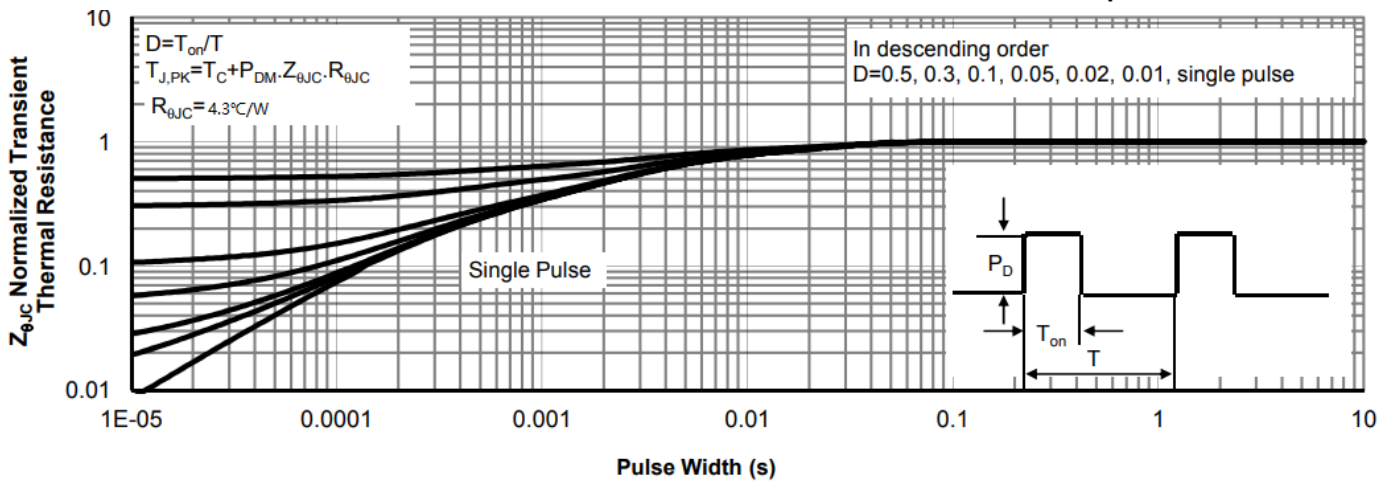
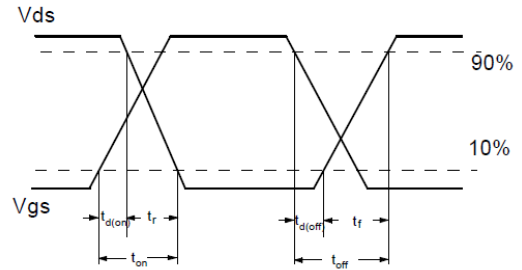
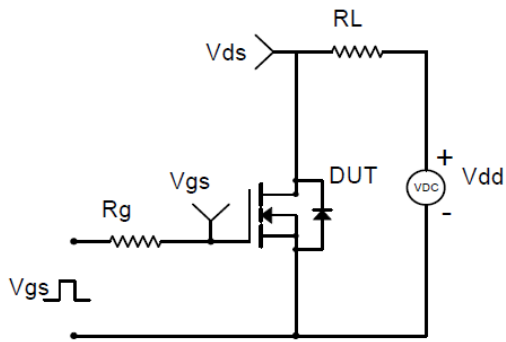
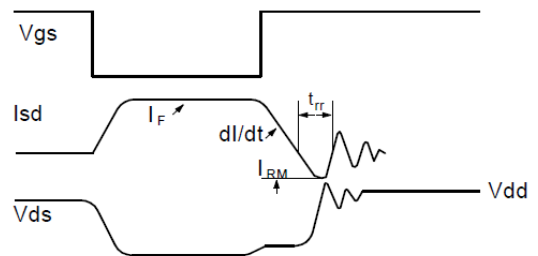
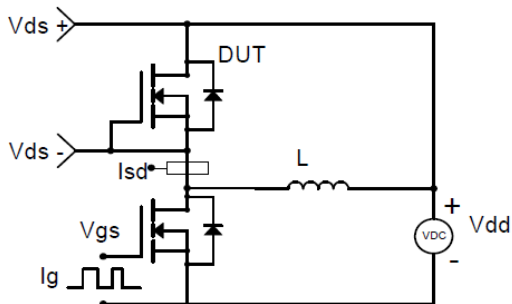


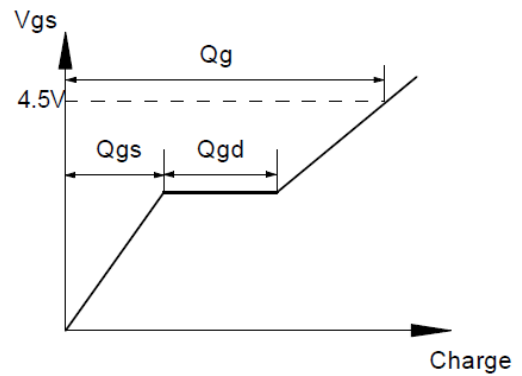
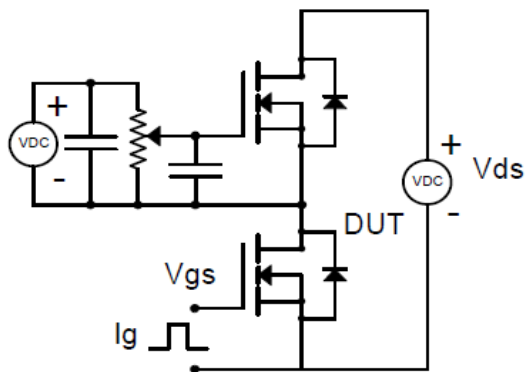
Figure9. Normalized Maximum Transient Thermal Impedance



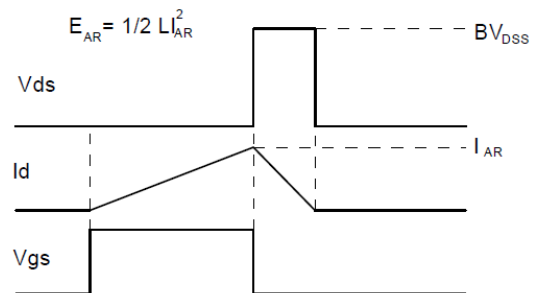
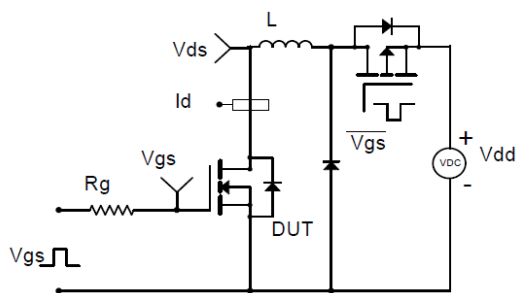
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

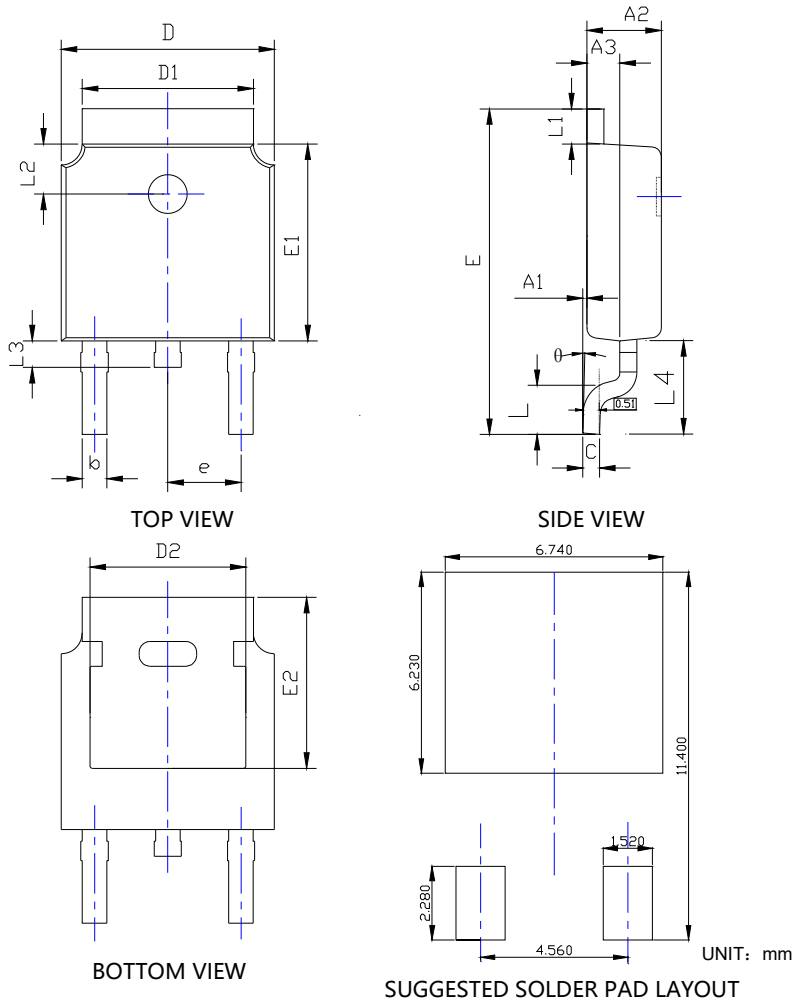


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJD60N02A

## ■ TO-252-B Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
$\theta$	0°	---	10°	0°	---	10°

### NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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